CMOS buffer delivers precise current pulses

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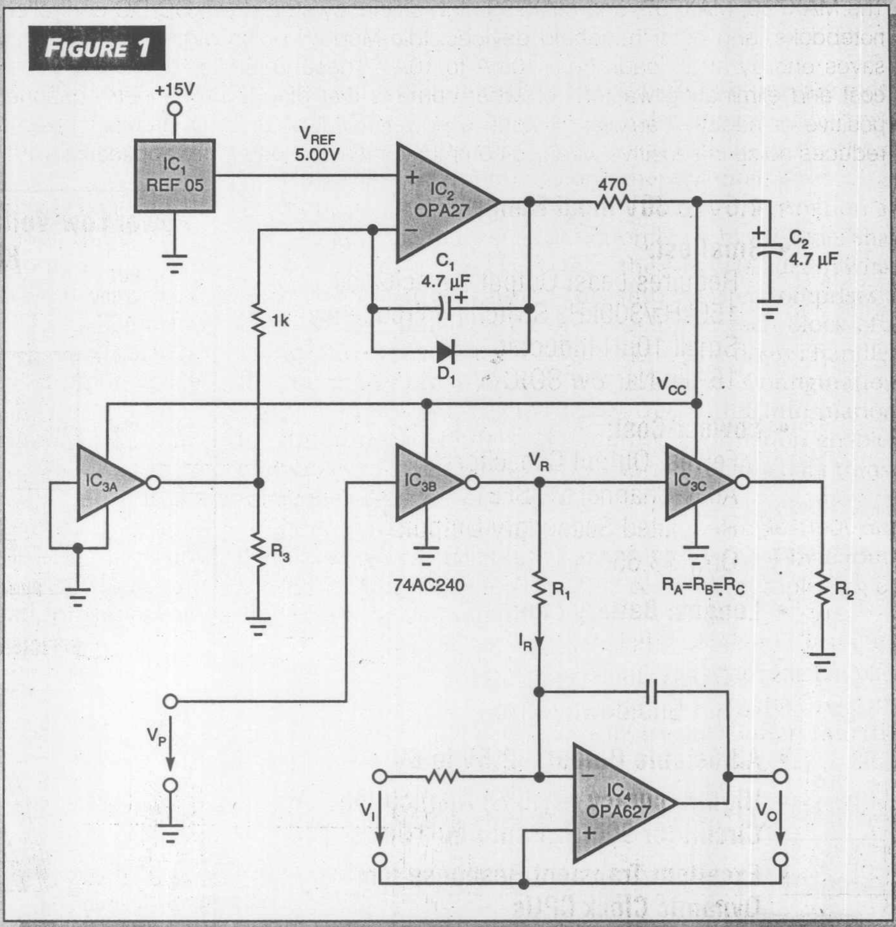
The circuit in Fig 1 delivers stable, fast-settling reference-current pulses. You can use the circuit in systems employing A/D, D/A, or V/F converters.

Digital input pulses, V_P, connect to IC_{3B}, a 74AC240 buffer. The 5.00V reference, IC_1, constrains IC_{3B}'s output, V_R, to either V_{REF} or 0V. IC_{3B}'s rise and fall times are <3 nsec. Resistor R_1 converts the voltage at the output of IC_{3B} to a current: $I_R=V_R/R_1$. I_R flows into integrator IC_4's virtual ground.

An analog control loop comprising IC_2 and IC_{3A} stabilizes V_{REF}. The loop compensates for the 20Ω output resistance of buffer IC_{3B}. And, the loop reduces high-frequency noise from reference IC_1 (Ref 1). Diode D_1 prevents reverse polarity during power-up.

You should use tantalum capacitors for C_1 and C_2. Locate C_2 as close as possible to IC_3's supply pins. If you use a low-temperature-coefficient Vishay (Malvern, PA, (610) 644-1300) resistor for R_1 and select 100 kΩ as the values for R_1, R_2, and R_3, IC_1 is the source of most of your current drift. (DI # 1635) EDN

FIGURE 1



This circuit delivers stable, fast-settling reference-current pulses because of its stable components and controlled-voltage level.

Reference

1. *Application note AB-003*, Burr-Brown Corp, Tucson, AZ. (602) 746-1111.

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Repeating one-shot yields clean, stable pulses

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Now and then, you need a repeating one-shot, such as a *multi-shot.* For example, when an input logic signal or alarm condition occurs, you may need an immediate pulse to provoke a sequence that eventually resets the condition. But, if the resetting fails, you need to keep generating pulses until the message gets through. If you give up sending pulses, something as important as an entire space mission could have to wait for an automatic reset.

Although you can generate multiple reset pulses many ways, most methods are fraught with annoyances. The first pulse can be twice as long as the follow-on pulses. Or, as for the retriggerable one-shot, keeping the pulse generator on prolongs the pulse instead of making new ones. When turned off, the pulse generator sometimes cuts the last output pulse off, hatching short glitches.

The circuits in Fig 1a and 1b are gated Schmitt oscillators. The oscillators respond to a negative input by producing a pulse of fixed length, regardless of how long the input stays on. The oscillators refuse to operate for a certain period. If the input is still there, the devices produce another pulse of the same fixed length.

In its quiescent state, the signal at the junctions is high (Fig 1a). C_1 couples the high-going transient to the diodes when the output toggles. The diodes clip the signal to 0.6V

above the positive rail. A relaxation cycle begins as C_1's charge drains away, and its voltage heads for the Schmitt trigger's *lower* threshold.

When the circuit receives a continuous input signal, each subsequent relaxation cycle starts with the diodes driven high. The diodes start high, even through C_1's voltage decays to the upper Schmitt level during the output pulse's on period. So, the circuit generates almost exactly the same pulse length every time, including the first time.

Fig 1b's circuit, the simpler of the two versions, lacks clamping diodes and a transistor. The circuit's first pulse is slightly longer because the transition starts at a higher voltage. **Fig 1b**'s circuit is a trifle less temperature-stable than Fig 1a's. (DI #1636) EDN

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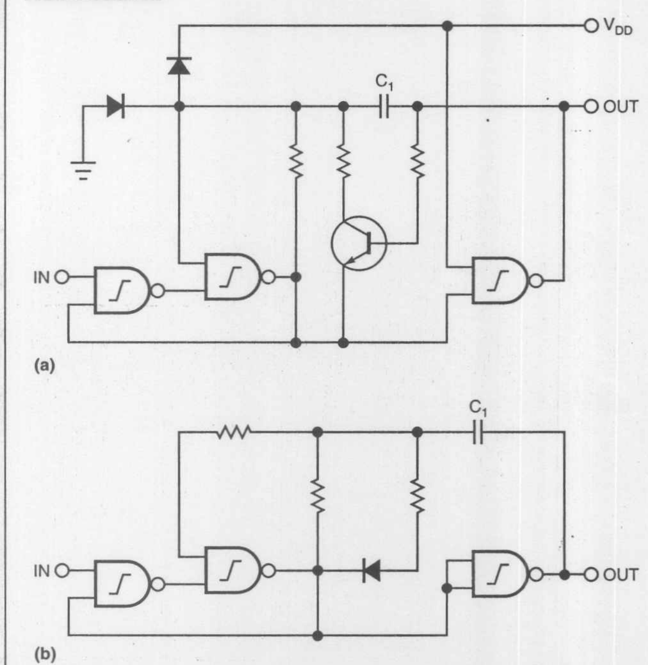
FIGURE 1



The gated Schmitt pulse generators in (a) and (b) respond to a negative input by producing a train of pulses of the same length.

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